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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HAN, CLEMENCE S	

ART UNIT	PAPER NUMBER
2665	9

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,941	STACEY ET AL.	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1–12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. An initialed and dated copy of Applicant's IDS form 1449, Paper No. 6, is attached to the instant Office action.

Response to Amendment

2. Responsive to preliminary amendment received on March 15, 2004, amended claims 1–7 and new claims 9–12 are entered as requested.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 8–12 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaffe et al. (US Patent 5,410,727).

In regard to claim 8, Jaffe teaches a method of processing a plurality of data streams in a digital subscriber line (DSL) system, comprising the acts of: calculating a plurality of input addresses for said plurality of data streams based on a plurality of input base addresses and a plurality of input offset addresses (Column 7 Line 4–10); storing a plurality of data from said plurality of data streams

according to said plurality of input addresses (Column 9 Line 22–25); calculating a plurality of processor addresses for the stored plurality of data based on a plurality of processor base addresses and a plurality of processor offset addresses (Column 10 Line 7–10); processing, using a single instruction, the stored plurality of data according to said plurality of processor addresses (Column 10 Line 10–11); calculating a plurality of output addresses for the processed plurality of data based on a plurality of output base addresses and a plurality of output offset addresses; outputting the processed plurality of data according to said plurality of output addresses (Column 10 Line 56 – Column 11 Line 6); and updating said plurality of input base addresses, said plurality of processor base addresses, and said plurality of output base addresses (Column 7 Line 15–23).

In regard to claim 9, Jaffe teaches a single instruction, multi data (SIMD) architecture for controlling the processing of plurality of data streams, comprising: a memory 330 that stores data from said plurality of data streams received from a plurality of channels; a processor 120, operatively coupled with said memory, that processes said data from said plurality of data streams; and a controller 370 that controls said processor, wherein storing said data in said memory de-couples a first operating rate of said processor and a second operating rate of said plurality of channels.

In regard to claim 10, Jaffe teaches said plurality of data streams carried in respective ones of said plurality of channels (Column 5 Line 59–66).

In regard to claim 11, Jaffe teaches a method of controlling processing of multiple data streams in a single instruction, multi data (SIMD) architecture, comprising the steps of: storing data in a memory as said data is received (Column 9 Line 22–25); at regular intervals, determining whether all of said data has been received; providing a signal indicating that all of said data has been received (Column 8 Line 13–35); using said signal to determine which of said data to process (Column 10 Line 7–10); and processing said data in accordance with said signal (Column 10 Line 10–11).

In regard to claim 12, Jaffe teaches said multiple data streams are carried in respective ones of a plurality of channels (Column 5 Line 59–66).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1–7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaffe et al. in view of Morton (US Patent 5,822,606).

In regard to claim 1, Jaffe teaches a single instruction, multiple data (SIMD) controller for processing a plurality of data streams in a digital subscriber line (DSL) system, comprising: a plurality buffer circuits 330 that store data from said plurality of data streams; a plurality of address generation circuits 350 that access said data stored in said plurality of circular buffer circuits; a plurality of processor circuits 120 that process said data accessed by said plurality of address generation circuits; and a program control unit 370 that controls said plurality of processor circuits with an instruction. Jaffe, however, does not teach the circular buffer. Morton teaches the circular buffer (Column 12 Line 58 – Column 13 Line 12). It would have been obvious to one skilled in the art to modify Jaffe to use the circular buffer as taught by Morton in order to process real–time data (Column 13 Line 8–12).

In regard to claim 2, Jaffe teaches a first section 310 that stores one or more symbols before being processed; a second section 140 that stores said one or more symbols being processed; and a third section 310 that stores said one or more symbols after being processed.

In regard to claim 3, one of said plurality of address generation circuits comprising a symbol manager circuit that generates an input base address, a processor base address, and an output base address, wherein said one of said

plurality of address generation circuits further receives an input offset address, a processor offset address, and an output offset address, and generates an input address, a processor address, and an output address in accordance with said input base address, said processor base address, and said output base address (Column 6 Line 61 – Column 7 Line 23).

In regard to claim 4, Jaffe teaches said plurality of processor circuits further receive a plurality of enable signals and selectively process said data based on said plurality of enable signals (Column 8 Line 13–35).

In regard to claim 5, Jaffe teaches said plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon whether a full symbol is ready for processing in each of said plurality of address generation circuits (Column 8 Line 13–35).

In regard to claim 6, Jaffe teaches said plurality of processor circuits further receive said plurality of enable signals and to selectively process said data based on said plurality of enable signals (Column 8 Line 13–35).

In regard to claim 7, Jaffe teaches said plurality of address generation circuits further selectively generate a plurality of enable signals, depending upon a difference between an input base address and a processor base address in each of said plurality of address generation circuits (Column 8 Line 13–35).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art with respect to the memory in general.

U.S. Patent 6,330,657 to Col et al.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (703) 305-0372. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (703) 308-6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C.H.

Clemence Han
Examiner
Art Unit 2665

HUY D. VU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600